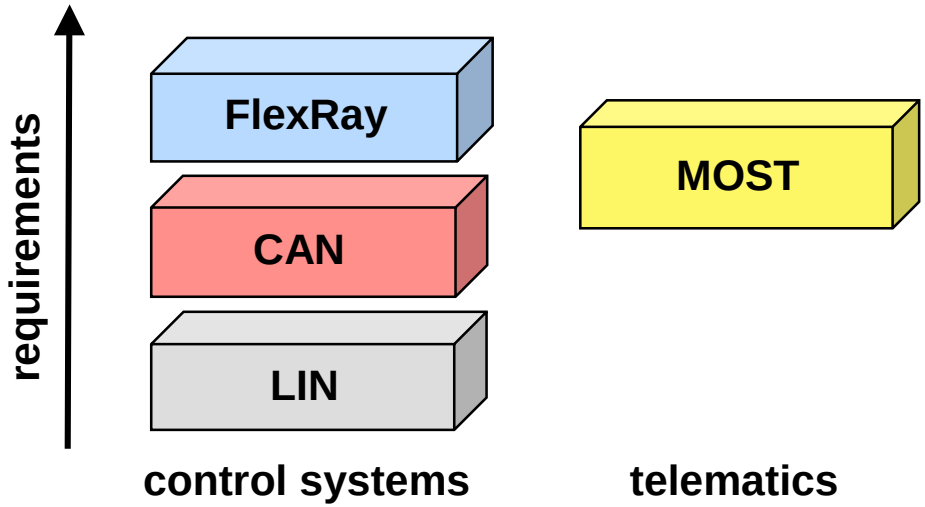
Advanced Automotive Communication System

Outline:

- **Scalable static and dynamic message transmission (deterministic and flexible)**
- **High net data rate of 5 Mbit/sec; gross data rate approximately 10Mbit/sec**
- **Scalable fault-tolerance (single and dual channel)**
- **Error containment on the physical layer through an independent Bus Guardian**
- **Fault tolerant clock synchronisation (global time base)**

Motivation

- Demand for a bus system with high data rate
- Deterministic and fault tolerant bus system for advanced automotive control applications
- Support from the bus system for distributed control systems
- Limited number of different communication systems within vehicles



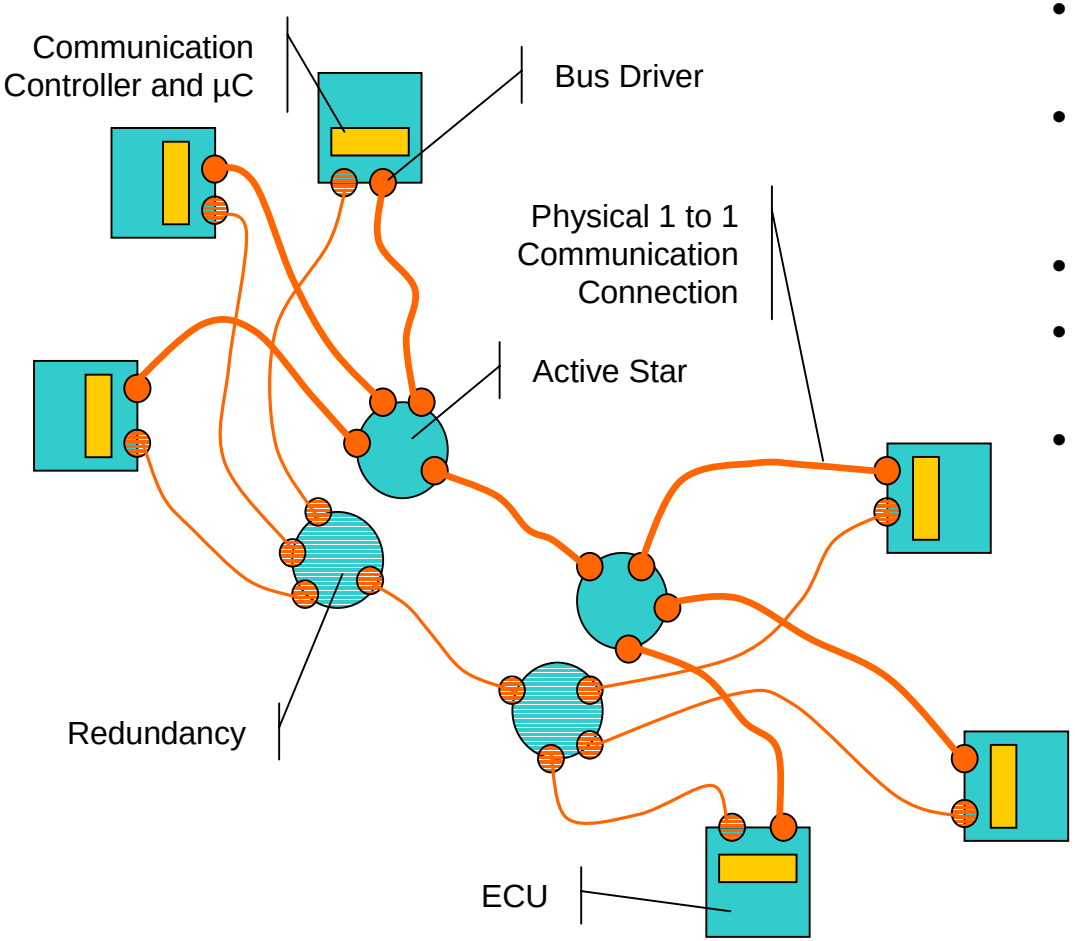
Goals

- **Develop an advanced communication technology for high-speed control applications in vehicles**
- **Make the technology available in the market place for everyone**
- **Drive the technology as a defacto standard**

Basic Features

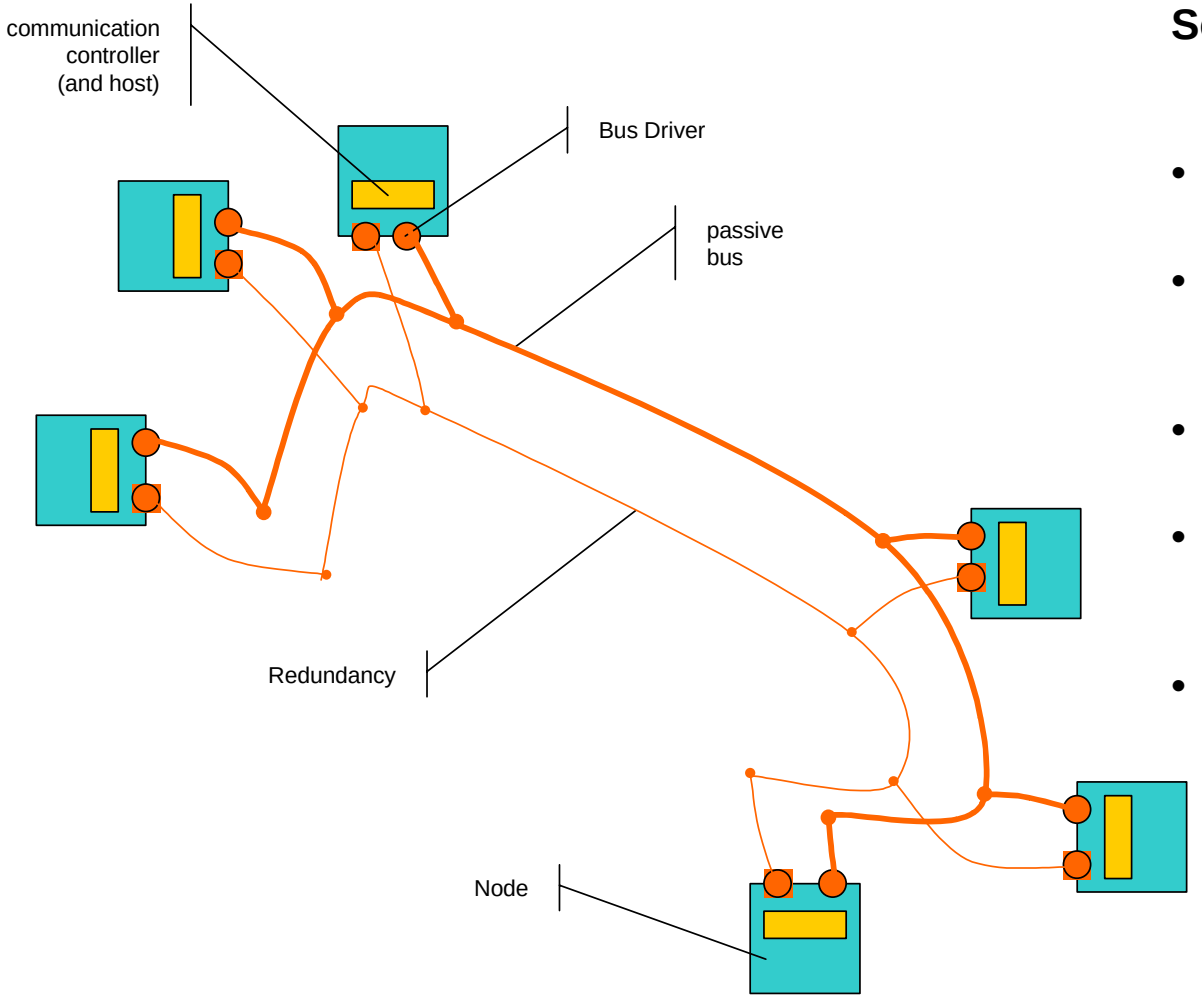
- Synchronous and asynchronous data transmission (scalable)
- High net data rate of 5 Mbit/sec; gross data rate approximately 10Mbit/sec
- Deterministic data transmission, guaranteed message latency and message jitter
- Support of redundant transmission channels
- Fault tolerant and time triggered services implemented in hardware
- Fast error detection and signalling
- Support of a fault tolerant synchronised global time base
- Error containment on the physical layer through an independent “Bus Guardian”
- Arbitration free transmission
- Support of optical and electrical physical layer
- Support for bus, star and multiple star topologies

Hardware Features and Topology of a Distributed FlexRay System - Active Star



- **Optional redundant communication channels**
- **1 to 1 communication connections in combination with active stars**
- **Support of “wake-up” via bus**
- **Support of net data rates up to 5 Mbit/sec**
- **Support of power management**

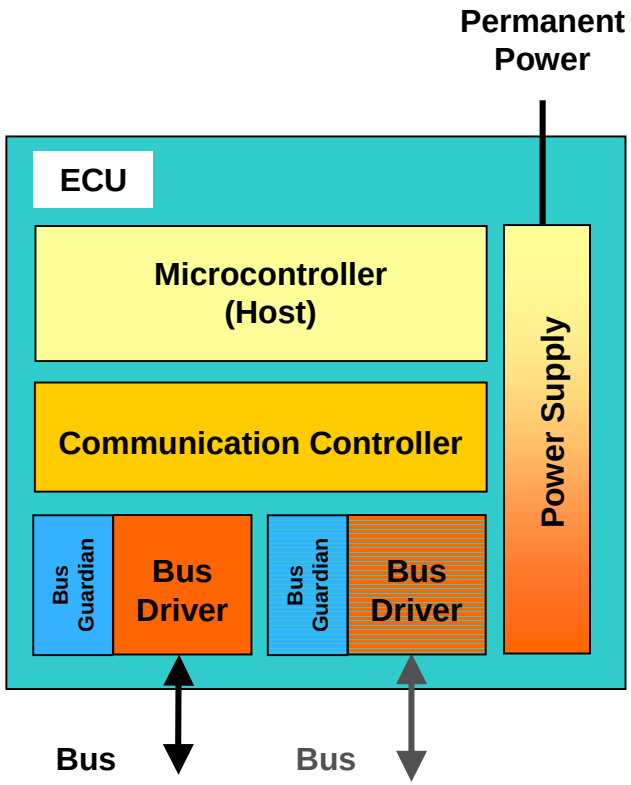
Hardware Features and Topology of a Distributed FlexRay System - Passive Bus



Solution with restrictions (reuse of available Physical Layer):

- **Optional redundant communication channels**
- **Support of “wake-up” via bus, depends on the Physical Layer**
- **low gross data rate (similar to CAN)**
- **Support of power management, depends on the Physical Layer**
- **Bus Guardian, depends on the Physical Layer**

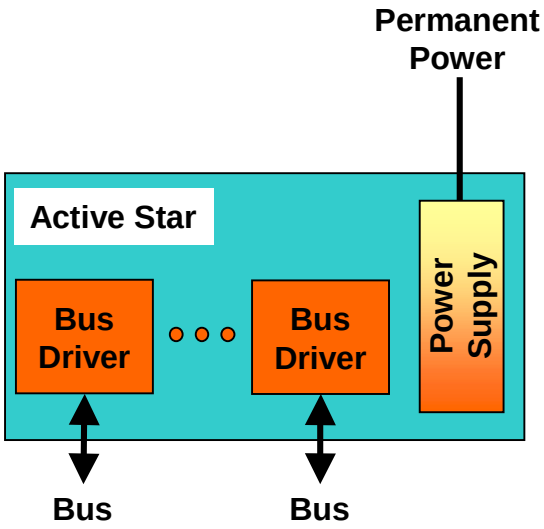
Features and Block Diagram of a FlexRay ECU



- **1 or 2 bus drivers connected to one communication controller**
- **Connection to “permanent power”**
- **“Wake-up” via bus**
- **“Shut-down” by the ECU**

Power modes of nodes	Communication	Power supply (internal)
Level 1	available	available
Level 2	unavailable	available
Level 3	unavailable	unavailable

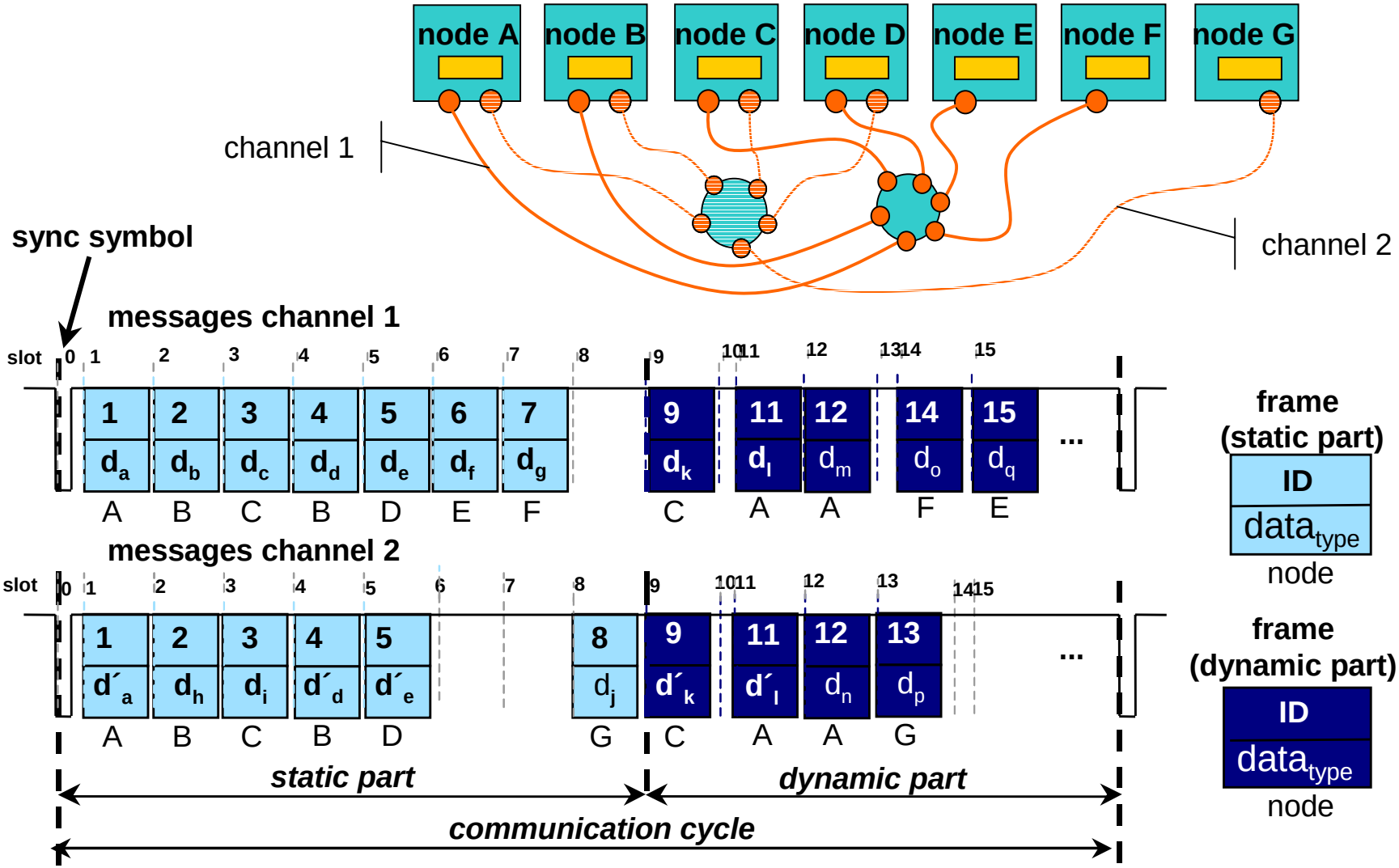
Features and Block Diagram of a FlexRay Active Star



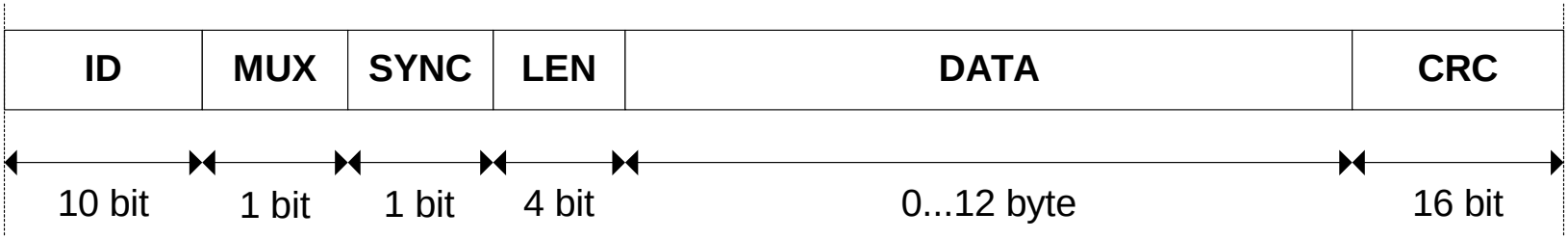
- **More than 1 bus driver required**
- **Communication controller and micro controller are not required**
- **Connection to “permanent power”**
- **“Wake-up” via bus**
- **“Shut-down” via bus**

Power modes of an active star	Communication	Power supply (internal)
Level 1	available	available
Level 2	unavailable	available
Level 3	unavailable	unavailable

Data Transmission



FlexRay Protocol Frame Format (I)



ID: Identifier, 10 bit, range: (1_{10} ... 1023_{10}), defines the slot number in the static part or the priority in the dynamic part

MUX: Multiplex Field, 1 bit, enables a node to transmit different messages with the same ID

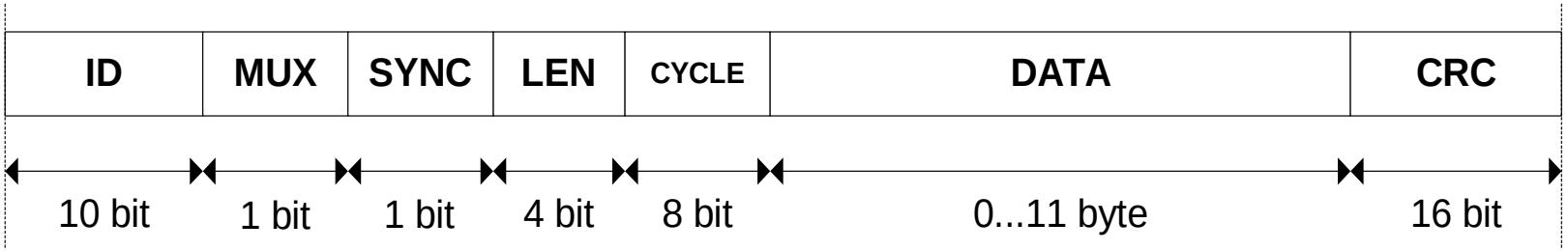
SYNC: Synchronisation Field, 1 bit, tags the frames which will be used for the clock synchronisation

LEN: Length field, 4 bit, LEN = number of used data bytes (0_{10} ... 12_{10})

D0 ... D11: Data bytes, 0-12 bytes

CRC: Cyclic Redundancy Check Field, 16 bit

FlexRay Protocol Frame Format (II)



The cycle counter will be used to synchronise application processes which are longer as the communication cycle.

CYCLE: Cycle Counter, 8 bit, range: (0_{10} ... 255_{10}). The CYCLE-field will be used as cycle counter or as a data byte. The cycle counter will be incremented consistently in all communication controllers at the beginning of each communication cycle

SYNC: Synchronisation field, 1 bit, tags the frames which contain the cycle counter

D0 ... D10: Data bytes, 0-11 bytes

FlexRay Protocol Clock Synchronisation

- **Synchronisation of the local clocks to a global time base**
- **Up to two asymmetric faults can be tolerated if there are a sufficient number of nodes**
- **Fault tolerant clock synchronisation is available in a pure static configuration and in a mixed configuration (static and dynamic part in the communication cycle)**
- **No fault tolerant clock synchronisation is available in a pure dynamic configuration**
- **Support of all topologies (single channel, dual channel, mixed single and dual channel)**
- **Only nodes in the static part can participate in the clock synchronisation (with frames which are tagged with the SYNC bit)**
- **All nodes can use the global time**